REMARKS

In response to the Office Action mailed September 7, 2006, and in view of the Request for Continued Examination filed concurrently herewith, Applicants respectfully request reconsideration. Claims 1-29 were previously pending in this application. Claims 6-29 have been canceled without prejudice or disclaimer. New claims 30-45 have been added. No claims have been amended herein. As a result, claims 1-5 are pending for examination with claims 1, 2, 30 and 42 being independent. No new matter has been added.

Objections to the Claims

The Office Action objected to claims 8 and 26. However, these objections are moot because claims 8 and 26 have been canceled.

Rejections Under 35 U.S.C. §102

The Office Action rejected claims 6-11, 13, 18-20 and 22 under 35 U.S.C. §102(e) as being anticipated by Choi, U.S. Patent No. 2003/0076332. However, these rejections are now moot because claims 6-29 have been canceled.

Rejections Under 35 U.S.C. §103

The Office Action rejected claim 1 under 35 U.S.C. §103(a) as being purportedly unpatentable over Richards (6,756,976) in view of Glennon (6,359,654), further in view of Wu, (6,414,689). The Office Action also rejected claims 2, 4 and 5 under 35 U.S.C. §103(a) as being unpatentable over Richards (6,756,976) in view of Glennon (6,359,654), in view of Leung, and further in view in view of Wu (6,414,689). Applicants respectfully traverse these rejections.

The Office Action concedes that neither Richards nor Glennon describes "for each row address of the frame memory, activating pixels of a screen line associated with said address offset by a same pixel position offset value, based on the read states of the row associated with said address" as recited in claim 1. However, the Office Action states alleges that Wu describes such a technique. Applicants respectfully disagree.

A. Discussion of Wu

Wu describes a technique for writing/reading pixel data to/from a frame memory. When blocks of data are to be written in the frame memory, the graphics engine (GE) 301 (FIG. 3) sends to the memory interface unit (MIU) 207 the address of the first data block location in the frame memory. When writing other data blocks, the GE does not send the entire addresses, but rather sends first and second address flag bits (ELO, AO) to reduce the amount of data exchanged. From the received flag bits EOL and AO, the MIU can compute the addresses of the frame memory where the following data blocks are to be written. Such a calculation is performed by a first offset value to the last calculated address when bit AO is equal to 1, or adding a second offset value to the starting address when bit EOL is equal to 1. Reading occurs in a similar manner to Wu's writing technique. Thus, Wu describes a technique for reducing the amount of address information that is exchanged when accessing a location in memory (Col. 3, line 54 - Col. 4, line 5). In Wu's device, each pixel of the screen is associated with a dedicated memory location in frame memory (Col. 9, lines 17-20).

B. The Claims Distinguish Over the References

Wu's address bit flags are an encoding technique for reducing the amount of address data that needs to be sent when exchanging address locations to be accessed in memory. In Wu's device there is a direct correspondence between the displayed image and the image stored in the frame memory, and their positions are not offset relative to one another. Therefore, although addresses are accessed using an offset value instead of the full address, the address locations that are accessed remain the same, and correspond directly to the displayed image.

By contrast, claim 1 recites, *inter alia*, "activating pixels of a screen line associated with said address offset by a same pixel position offset value." Wu does not teach or suggest such a limitation. Rather, Wu's device displays the image in the same way that it is stored in the frame memory. Richards and Glennon fail to remedy this deficiency of Wu. Therefore, claim 1 patentably distinguishes over the combination of Richards, Glennon and Wu. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 2 recites, *inter alia,* a dedicated address circuit receiving the address of the row read by the read means and transmitting to the row driver a new address corresponding to the address of the read row offset by a same pixel position offset value. As should be appreciated from the

above discussion with respect to claim 1, Wu does not teach or suggest this limitation. Richards, Glennon and Leung fail to remedy this deficiency of Wu. Therefore, claim 2 patentably distinguishes over the combination of Richards, Glennon, Leung and Wu. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 3-5 depend from claim 2 and are therefore patentable for at least the same reasons.

New Claims

New independent claim 30 recites, *inter alia*, a second memory [that] shifts storage locations at which the row of image data is stored based on the column offset value such that the row of image data is stored in second storage locations of the second memory, the second storage locations being shifted with respect to the first storage locations. The references relied upon in the Office Action do not teach or suggest a memory that shifts storage locations of a row of image data as claimed. Therefore, claim 30 and claims 31-41 depending therefrom patentably distinguish over the references relied upon in the Office Action.

New independent claim 42 recites, *inter alia*, a logic unit [that] receives a first row address corresponding to a row of the image data and performs an operation on the first row address using the row offset value to determine a second row address that is offset from the first row address. The references relied upon in the Office Action do not teach or suggest a logic unit that determines a second row address as claimed. Therefore, claims 42 and 43-45 depending therefrom patentably distinguish over the references relied upon in the Office Action.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

By: _____

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